## REMARKS

Claims 1, 3, 5-12, 14, 15, 17, 18, 20 and 24-31 are pending in the application.

Claims 1 and 24-28 were rejected under 35 U.S.C. § 103(a).

Claims 3, 5-12, 14, 15, 17, 18, 20 and 29-31 were rejected under 35 U.S.C. 103(a).

### *Interview Summary*

Applicant thanks the Examiner for the telephone interview conducted between the Examiner and Applicant's representative, Brian Wichner, on December 6, 2006. Before the interview, applicant sent arguments to the Examiner explaining several reasons for allowability of the claims. During the interview, the Examiner acknowledged that those reasons appear persuasive. These reasons are included below.

### *Claim Rejections – 35 U.S.C. § 103*

Claims 1 and 24-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Deering (US005544306A) in view of Devic (US005812138A).

Claims 1, 12 and 28 (the independent claims) each recite a transfer of the external depth data, via the connecting line, into the memory cell array.

The Examiner, acknowledging that Deering does not teach the above recitation, relies on Devic. But Devic fails to teach transferring the external depth data, via the connecting line, into the memory cell array, as now explained.

Devic, in FIG. 5, shows a write enable signal as the only connecting line from the compare circuit 510 and the memory cell array 400. Claims 1, 12 and 28 require the data itself to be written through this line. Instead the updated z data is written via the 32-bit wide line from the z interpolator 410 directly to the memory 400. A write enable cannot transfer the z data because it is only one-bit wide, for example. See FIG. 5 again for the write enable signal 455 from the OR gate 450, which shows explicitly that a write enable signal is one-bit wide.

Because Devic fails to make up for Deering's shortcomings, their combination fails to teach each and every limitation of the claims.

In rejecting claim 28, the Examiner says that element 114 in FIG. 4 of Deering is the control circuit of the claim, and that 70 is the memory controller. If this is true then claims 24 through 27 are allowable because claims 24 and 26 recite control pins that *directly* connect the

compare circuit 58 to the memory controller 70. But Deering does not show this direct connection because all control lines (such as 178) go through control circuit 114. Lines that appear not to go through the control circuit 114 are PA_DX and PA_DQ. But these are not control signals (as in claims 25 and 27) but instead are data lines (see Table 1 of Deering, for example).

Thus, in addition to being allowable based on their dependency on claim 1, claims 24-27 are novel in view of Deering for at least the reason above.

Claims 3, 5-12, 14, 15, 17, 18, 20 and 29-31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Deering (US005544306A) and Devic (US005812138A) in view of Dowdell (US005301263A).

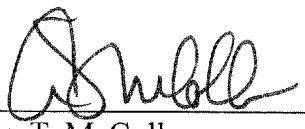
Claim 12 is novel in view of Deering and Devic, as explained above. Dowdell fails to make up for shortcomings of the other references.

The remaining claims are dependent on claims 1, 12 and 28, respectively, and are in condition for allowance based on their own novel features and the novelty of their base claims.

For the foregoing reasons, reconsideration and allowance of the claims of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

**Customer No. 20575**